REMARKS

With this amendment, claims 2-18 and 20-22 remain pending. Claims 21 and 22 has been amended. The amendments to claims 21 and 22 are supported by, for example, paragraph [0027] of the Specification.

The Applicant has carefully and thoughtfully considered the Office Action and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

Rejections under 35 U.S.C. § 103

On pages 2-14, the Action rejects claims 2-16 and 21-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 7,254,111 to Choe et al. (hereinafter Choe) in view of U.S. Published Patent Application No. 2003/0120876) to Hass et al. (hereinafter Hass). Applicants respectfully traverse these rejections.

With respect to claim 21, Applicants respectfully submit that Choe in view of Hass does not teach or suggest all of the elements of claim 21, as will be shown, for at least the following four reasons.

First, Choe does not disclose "a plurality of control buses which connect said processors to each other," as recited in claim 21. Instead, Choe discloses a parallel router comprising a plurality of routing nodes and a switch fabric capable of transmitting message packets between a transmitting node and a receiving node. Choe, abstract and FIG. 2. The routing nodes and switch fabric are interconnected via high-speed links. Choe, col. 5, l. 62-64. Each routing node contains an input-output processor (IOP) and one or more physical medium devices (PMD). Choe, col. 5, l. 30-24 and FIG. 2. Each IOP buffers incoming Internet protocol (IP) packets, classifies requested services, looks up destination addresses from packet headers, and forwards packet to the outbound IOP. Choe, col. 5, l. 42-55. Moreover, each IOP also maintains an internal routing table determined from routing protocol packets and computes the shortest data paths from the routing table. *Id.*

Thus, Choe teaches a network of routing nodes and a switch fabric, interconnected via high-speed internal links, in which each node is controlled by a routing table stored in each routing node. Choe does not teach or suggest the presence of, or need for, "a plurality of control buses" in addition to the high-speed internal links between the routing nodes and the switch fabric. Choe, therefore, fails to teach or suggest "a plurality of **control buses** which connect said processors to each other," as recited in claim 21.

Furthermore, Hass fails to overcome the deficiencies of Choe. Hass discloses a multi-processor unit includes a set of processing clusters where each cluster is coupled to a data ring and a snoop ring. Hass, abstract. However, neither the data ring or the snoop ring of Hass is equivalent to "a plurality of control buses which connect said processors to each other," as recited in claim 21. The combination of Choe and Hass, therefore, fails to teach or render obvious "a plurality of control buses which connect said processors to each other," as recited in claim 1.

Second, Choe does not disclose "a plurality of control buses [] wherein said control buses have a lower communication speed than that of said internal communication path," as recited in claim 21. Instead, as discussed above, Choe discloses a parallel router comprising a plurality of routing nodes and a switch fabric capable of transmitting message packets between a transmitting node and a receiving node. Choe, abstract and FIG. 2. The routing nodes and switch fabric are interconnected via high-speed links. Choe, col. 5, l. 62-64. Each routing node contains an input-output processor (IOP) and one or more physical medium devices (PMD). Choe, col. 5, l. 30-24 and FIG. 2. Each IOP buffers incoming Internet protocol (IP) packets, classifies requested services, looks up destination addresses from packet headers, and forwards packet to the outbound IOP. Choe, col. 5, l. 42-55. Moreover, each IOP also maintains an internal routing table determined from routing protocol packets and computes the shortest data paths from the routing table. *Id.*

Thus, Choe teaches a network of routing nodes and a switch fabric, which are **interconnected via high-speed internal links**, in which each node is controlled by a routing table stored in each routing node. Choe does not teach or suggest the presence of, or need for, "a plurality of control buses" that are slower than, the high-speed internal links of FIG. 2. Choe,

therefore, fails to teach or suggest "a plurality of control buses [] wherein said control buses have a lower communication speed than that of said internal communication path," as recited in claim 21.

Furthermore, Hass fails to overcome the deficiencies of Choe. Hass discloses a multi-processor unit includes a set of processing clusters where each cluster is coupled to a data ring and a snoop ring. Hass, abstract. However, neither the data ring or the snoop ring of Hass is equivalent to "a plurality of control buses [] wherein said control buses have a lower communication speed than that of said internal communication path," as recited in claim 21. The combination of Choe and Hass, therefore, fails to teach or render obvious "a plurality of control buses [] wherein said control buses have a lower communication speed than that of said internal communication path," as recited in claim 1.

Third, Choe does not disclose "a plurality of processors []; a plurality of processor interfaces having one or more cell distributors and one or more selectors," as recited in claim 21. In rejecting claim 21, the Office Action aligns the recited limitation with the routing nodes of Choe, Choe, FIG. 2. Applicant disagrees with this alignment.

As discussed above, Choe discloses a parallel router comprising a plurality of routing nodes and a switch fabric capable of transmitting message packets between a transmitting node and a receiving node. Choe, abstract and FIG. 2. The routings node and switch fabric are interconnected via high-speed links. Choe, col. 5, l. 62-64. Each routing node contains an IOP and one or more PMD. Choe, col. 5, l. 30-24 and FIG. 2. Each IOP buffers incoming Internet protocol (IP) packets, classifies requested services, looks up destination addresses from packet headers, and forwards packet to the outbound IOP. Choe, col. 5, l. 42-55. Each PMD frames an incoming packet from an IP network to be processed in an IOP and performs bus conversion functions. Choe, col. 5, l. 52-55.

However, the IOP and PMD of Choe are not equivalent to the cell distributors and selectors of claim 1. Thus, Choe does not teach or suggest the presence of, or need for, "processor interfaces having one or more cell distributors and one or more selectors" in addition to the IOP and PMDs contained in each routing node. Choe, therefore, fails to teach or suggest "a plurality of

processors []; a plurality of processor interfaces having one or more cell distributors and one or more selectors," as recited in claim 21.

Furthermore, Hass fails to overcome the deficiencies of Choe. Hass discloses a multi-processor unit includes a set of processing clusters where each cluster is coupled to a data ring and a snoop ring. Hass, abstract. However, neither the data ring or the snoop ring of Hass is equivalent to "a plurality of processors []; a plurality of processor interfaces having one or more cell distributors and one or more selectors," as recited in claim 21. The combination of Choe and Hass, therefore, fails to teach or render obvious "a plurality of processors []; a plurality of processor interfaces having one or more cell distributors and one or more selectors," as recited in claim 1.

Fourth, Choe does not disclose "cell distributors [] coupled to receive communication cells from said internal communication path and output said communication cells onto said internal communication path when the destination of said received communication cells is not to the corresponding processor," as recited in claim 21. In rejecting claim 21, the Office Action aligns the recited limitation with the linking of the routing nodes with the switch fabric of Choe. Choe, FIG. 2. Applicant disagrees with this alignment.

As discussed above, Choe discloses a parallel router comprising a plurality of routing nodes and a switch fabric capable of transmitting message packets between a transmitting node and a receiving node, via a switch fabric. Choe, abstract and FIG. 2. The routing nodes and switch fabric are interconnected via high-speed links. Choe, col. 5, l. 62-64. Each routing node contains an IOP and two PMDs. Choe, col. 5, l. 30-24 and FIG. 2. Each PMB is connected to one or more subnets or adjacent routers but only a single IOP. Choe, col. 5, l. 42-44 and FIG. 2. Each IOP is connected to a single PMD and the switch 249. Choe, col. 5, l. FIG. 2. In operation, each PMD of a transmitting node frames an incoming packet from an IP network and sends it to the one and only IOP to which it is connected (i.e. the corresponding processor). Choe, col. 5, l. 52-55 and FIG. 2. Thus, the PMD in a transmitting node of Choe cannot send a packet to an IOP that does not correspond to it. Choe, therefore, fails to teach or suggest "cell distributors [] coupled to receive communication cells from said internal communication path and output said communication cells

onto said internal communication path when the destination of said received communication cells is not to the corresponding processor," as recited in claim 21.

Furthermore, Hass fails to overcome the deficiencies of Choe. Hass discloses a multi-processor unit includes a set of processing clusters where each cluster is coupled to a data ring and a snoop ring. Hass, abstract. However, neither the data ring or the snoop ring of Hass is equivalent to "cell distributors [] coupled to receive communication cells from said internal communication path and output said communication cells onto said internal communication path when the destination of said received communication cells is not to the corresponding processor," as recited in claim 21. The combination of Choe and Hass, therefore, fails to teach or render obvious "cell distributors [] coupled to receive communication cells from said internal communication path and output said communication cells onto said internal communication path when the destination of said received communication cells is not to the corresponding processor," as recited in claim 1.

For at least the reasons set forth above, Applicants believe that claim 21 is allowable and respectfully request that the above rejection of claim 21 be withdrawn and that claim 21 be allowed.

Dependent claims 2-18 and 20 are believed to be allowable, at least, for being dependent from an allowable claim. Therefore, Applicants respectfully request that the above rejection of claims 2-18, 20, and 21 be withdrawn and that claims 2-18, 20, and 21 be allowed.

Claim 22 contains material that is similar to claim 21 and is therefore allowable for the same reasons. Therefore, Applicants respectfully request that claim 22 be allowed.

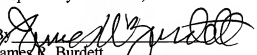
Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Dated: 3/30/2009

Respectfully submitted,

By 
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